33.7 A sub-1.5°$_{rms}$ Phase-Noise Ring-Oscillator-Based Frequency Synthesizer for Low-IF Single-Chip DBS Satellite Tuner-Demodulator SoC

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Most existing DBS tuners [1, 2, 3] use a direct-conversion architecture that requires a low frequency step in the synthesizer. This can be achieved either with a single-loop LC-oscillator-based PLL [1, 2] or with cascaded PLLs [3]. A large number of LC oscillators are used in [1] to cover the wide satellite-TV spectrum, but drawbacks include large die area due to on-chip planar inductors and high sensitivity to magnetic noise coupling and frequency pulling. In [2], a size reduction is achieved by using only two LC oscillators and switching different capacitor banks to cover the wide frequency range; this comes at the price of degraded phase noise. A higher complexity dual-loop synthesizer is proposed in [3]. It uses an LC oscillator PLL to ensure fine frequency resolution, cascaded with a ring oscillator PLL to provide a wide frequency range. The stringent satellite-TV phase-noise specification (<2.8°$_{rms}$ for QPSK and <2°$_{rms}$ for 8-PSK modulation) requires a small loop-filter (LF) resistor, often leading to nF-range capacitors that are hard to integrate on-chip.

In this paper, a single-loop fully integrated 0.13µm CMOS ring-oscillator-based frequency synthesizer for low-IF DBS receivers is presented. Figure 33.7.1 shows the top-level diagram of the single-chip DBS tuner-demodulator. The chip uses an analog mixing stage that down-converts a cluster of channels to a low IF (30 to 50MHz), followed by a second mixing stage implemented in the digital demodulator that performs the final channel selection. The low-IF tuner architecture does not increase circuit complexity since the second digital mixing is also required in the direct-conversion case to compensate for outdoor LNB oscillator temperature variations. A low-IF tuner can tolerate a wide frequency step from the synthesizer, allowing its implementation with a wideband ring-oscillator-based PLL. Using a ring oscillator reduces the synthesizer die size by a factor of 5 to 10 and provides lower sensitivity to magnetic coupling compared to that of existing LC-based solutions [1, 2, 3]. The challenges in this design are higher noise and spur contribution from the PLL front-end due to the required wide loop bandwidth and the large oscillator gain.

The large tuning range and low supply voltage of deep-submicron CMOS lead to a very high oscillator gain (K_{vco}). Placing an attenuator (A_t) between the LF and the oscillator is equivalent to an oscillator gain reduction, which helps both front-end noise and spurs attenuation. For a given noise contribution from the LF, the attenuator allows the usage of a resistor A_t^2 times larger and therefore reduces the size of the LF capacitance by A_t^2, enabling its on-chip integration. Figure 33.7.2 shows the noise-attenuating LF principle together with its circuit implementation. A passive-RC LF(C_i, R, C_p) is used due to its excellent supply-noise rejection. The attenuator is realized with a resistor divider R_{d1}, R_{d2}, that needs to be buffered from the high-impedance node of the LF to avoid reference spurs degradation. To minimize the required headroom voltage, a zero-V_T thick-oxide NFET M_{fol} is used as a source-follower buffer. A dedicated high PSRR regulator (OA_{reg}, M_{reg}) reduces the supply spurs coupling into the LF, and a zero-V_T FET active-RC filter (R_l, C_l, M_l) provides further supply-spur attenuation. To minimize the required headroom voltage and thus increase the achievable attenuation factor, a diode device M_{off} is connected in series with the resistor divider to generate the minimum control-voltage value (0.5 V). The divider uses a moderate bias current to reduce R_{d1} and R_{d2} and minimize their noise contribution. The C_{p2} capacitor adds a fourth pole in the loop that further rejects high-frequency noise and spurs.

Figure 33.7.3 shows the top-level diagram of the proposed wideband PLL. Separate supplies are used for the digital and analog PLL blocks. To minimize the reference-clock phase-noise, the amplitude of the crystal oscillator is maximized by using a 3.3V supply with a dedicated R_xC_x filter that attenuates high-frequency supply tones. The reference-clock squaring buffer is biased from a low-noise V_T/R-based regulator that ensures both high forward and reverse PSRR. The PFD and its output buffers current spikes, are closed locally with a second regulator to minimize the spur contamination of the PLL supply and to reduce magnetic-loop area. Similarly, a high reverse PSRR regulator (R-PSRR) is used for the feedback divider (Div.N) to contain its large current spikes. The chopping action of the charge pump (CP) can down-convert high-frequency supply spurs into the RF PLL bandwidth, but a regulator cannot be used due to limited available headroom. Instead, a low-corner-frequency R_c,C_c filter is placed in series with the CP supply. To achieve a process-independent loop bandwidth and damping factor, the LF resistor is calibrated to an external high-precision resistor while the CP current (I_{cp}) is adjusted by an open-loop calibration that measures the VCO output frequency and sets a current DAC such that the K_{vco}.I_{cp} term remains constant.

In wide-bandwidth PLLs, the reference-clock path, as shown in Fig. 33.7.4, is a major contributor to output phase noise and spur performance. The nonlinear edge- squaring process of the crystal sine-wave can down-convert high-frequency noise and spurious tones from both supply and input signal lines of the squaring buffer into the PLL bandwidth. The crystal-oscillator bondwire picks up high-frequency tones from the high-current switching blocks of the demodulator (digital PLL, ADC and MPEG output buffers). Also, the high-frequency tones can couple to the RF PLL digital supply bondwire and thus modulate the squaring-buffer trip point. An R_fC_f filter is placed between the crystal oscillator and the squaring buffer to attenuate the high-frequency tones before they are down-converted by the nonlinear operation. The squaring buffer is biased from an open-loop regulator built with a low-noise V_T/R current injected into a replica diodes leg M_{d1}, M_{d2}. A large bypass capacitor C_{byp} ensures high PSRR.

Figure 33.7.5 shows the low-noise ring oscillator and its output buffers. Multi-GHz oscillators require small-size devices which results in large mismatches preventing a direct quadrature generation. A three-stage ring oscillator is used that generates a 2.24 to 4.48GHz output clock. A divide-by-two circuit, built with cross-coupled CML latches, provides quadrature outputs. To prevent the oscillator frequency from falling into the LNA input signal spectrum, a divide-by-four is used for LO frequencies lower than 1.12GHz. A low $1/f^3$ phase-noise is achieved by combining a PFET differential pair with a triode-mode NFET load. A low-noise high-PSRR series regulator is used to bias the oscillator and minimize the supply-injected spurs. The oscillator gain changes proportionally with the divider modulus (N) using switched-capacitor banks at the output of each ring inverter. This keeps the K_{vco}/N term constant, ensuring a divider-independent PLL damping factor and bandwidth. The R_{sh} shunt resistor in parallel with each inverter output decreases the oscillator gain, improving spur and noise performance, and also reducing the required bias current at maximum oscillating frequency. Each inverter has its own pseudo-differential output buffer to ensure symmetrical loading.

Figure 33.7.6 presents the measured output LO phase-noise together with the close-in and far-out LO frequency spectrum obtained at the maximum PLL frequency (2.24GHz = 4.48GHz/2) with the demodulator being active. The worst-case in-band phase noise is –98dBc/Hz while the ring-oscillator phase-noise is –100dBc/Hz @ 1MHz offset, achieving less than 1.5°$_{rms}$ double-sided integrated phase noise from 10kHz to 10MHz, which exceeds the specifications for 8-PSK DBS receivers. The reference spurs are less than –60dBc while the largest coupled spurs are lower than –50dB. The DBS frequency-synthesizer features a 20MHz frequency step, <40mA supply current from a 3.3V supply, and 0.3mm² die area. Figure 33.7.7 shows the die micrograph of the single-chip DBS tuner-demodulator.

References:

[1] A. Jayaraman, et al., "A Fully Integrated Broadband Direct Conversion Receiver for DBS Applications," *ISSCC Dig. Tech. Papers*, pp. 140-141, Feb., 2000.

[2] B. Kim, et al., "A 9dBm IIP3 Direct Conversion Satellite Broadband Tuner-Demodulator SoC," *ISSCC Dig. Tech. Papers*, pp. 446-447, Feb., 2003.

[3] C. Vaucher, D. Kasperkovitz, "A Wideband Tuning System for Fully Integrated Satellite Receivers," *IEEE J. Solid-State Circuits*, vol.33, no.7, pp. 987-997, July, 1998.

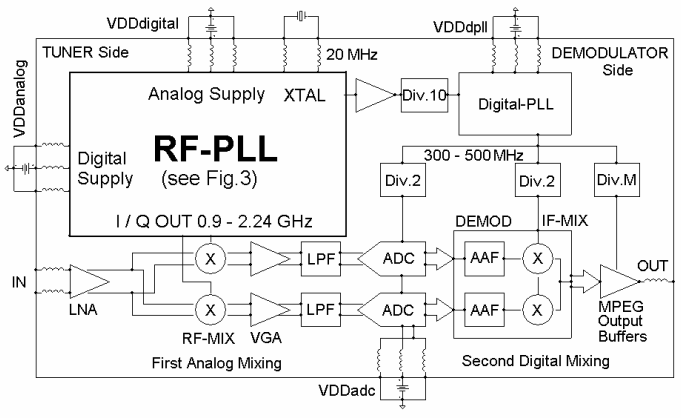

Figure 33.7.1: Single-chip low-IF DBS tuner-demodulator top-level diagram.

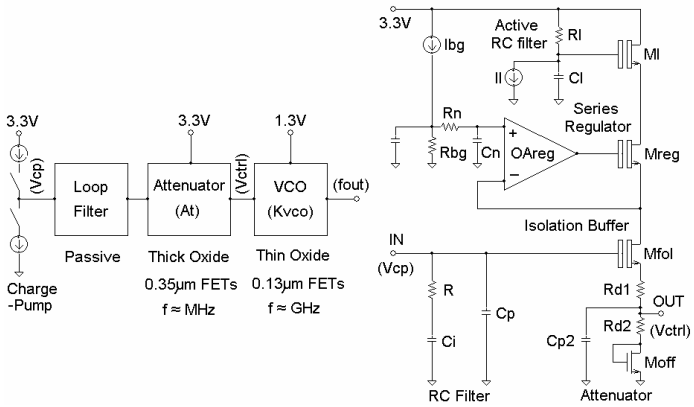

Figure 33.7.2: Noise attenuating loop filter principle and implementation.

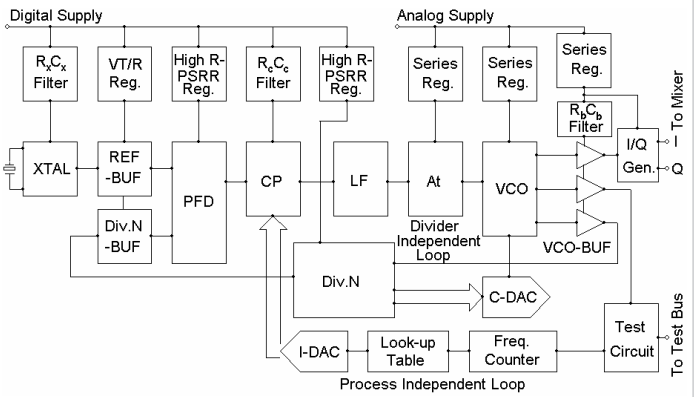

Figure 33.7.3: PLL top-level diagram with power-supply partitioning and regulation.

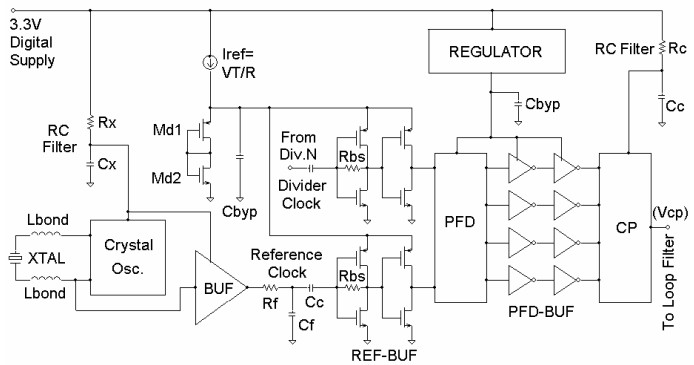

Figure 33.7.4: Reference path spurs reduction (XTAL, REF-BUF, PFD, PFD-BUF, CP).

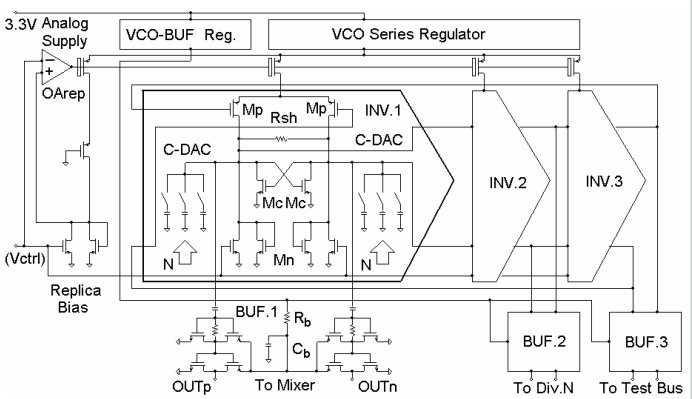

Figure 33.7.5: Low phase-noise VCO with shunt-resistor gain reduction.

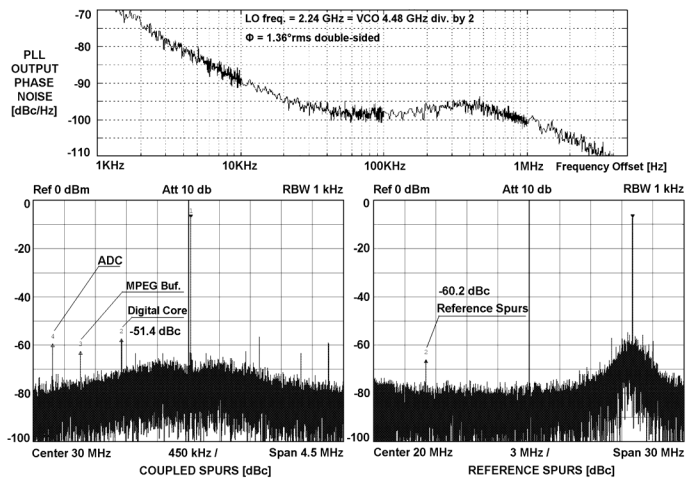

Figure 33.7.6: PLL phase noise, close-in and far-out frequency spectrum and spurs.

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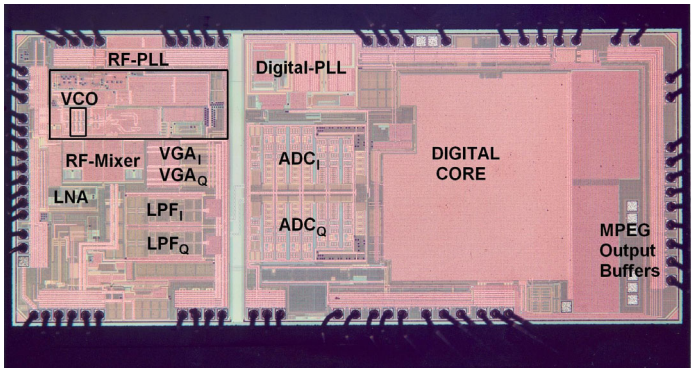

Figure 33.7.7: Single-chip DBS tuner-demodulator IC die micrograph.

